Here, the two CMOS gates are wired as a 100 Hz astable multivibrator that drives the lamp via Q_1-Q_2 and has its duty cycle or mark/space ratio fully variable from 1:20 to 20:1 via RV_1, thus enabling the mean power drive to the lamp to be varied from about 5 to 95 per cent of maximum via RV_1. Since the period of the 100 Hz waveform (10 ms) is short relative to the thermal time constant of the lamp, its brilliance can be varied from near-zero to maximum with no sign of flicker. Note that on/off switch S_1 is ganged to RV_1, so the circuit can be switched fully off by simply turning RV_1 fully anti-clockwise.

Manual clocking

In Chapter 7 we showed how simple clocked flip-flop ICs (such as the 4013B dual D-type) can be used as counter/dividers. One thing that we did not explain was how to clock these counters manually via a push-button switch. This omission is put right in *Figure 10.17*, which shows how to clock a single 4013B stage via S_1.

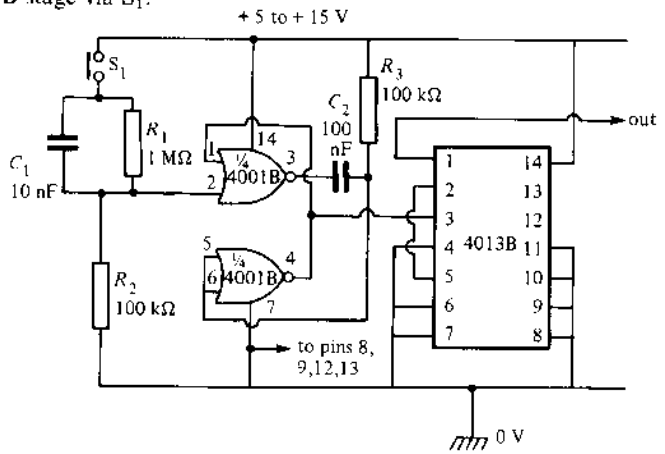

Figure 10.17 *Manual clocking of a 4013B counter/divider stage*

Here, the two 4001B gates are configured as a monostable multivibrator that generates a single 10 ms clock pulse each time S_1 is operated, thus causing the D-type flip-flop to change state; thus, S_1 must be operated twice to make the flip-flop go through a complete on/off or divide-by-two sequence. Note that the C_1-R_1 network effectively debounces S_1 and helps ensure clean triggering of the monostable circuit.

4046B PLL circuits

In Chapter 5 we introduced the 4046B phase-locked-loop (PLL) IC (see *Figure 5.25*) and showed how it can be used in voltage-controlled oscillator (VCO) applications. This chip actually contains two phase comparators, a wide-range VCO, a zener diode, and a few other bits and pieces, and is specifically intended for use in PLL applications such as automatic frequency tracking, frequency multiplication, and frequency synthesis.

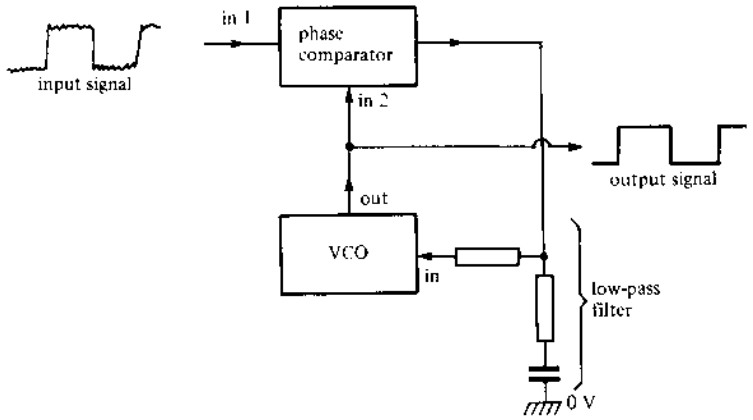

Figure 10.18 *Basic PLL frequency tracking circuit*

The basic operating principle of the PLL can be understood with the aid of the frequency tracking circuit of *Figure 10.18*. Here, the phase comparator element has two input terminals, one fed from an external input signal and the other from the output of the VCO element. The comparator compares the phase and frequency of the two inputs and generates an output proportional to their difference; this output signal is then smoothed via the low-pass filter network and fed to the control input terminal of the VCO, thus completing the phase-locked feedback loop.

The basic action of the above circuit is such that if the VCO frequency is below that of the external signal the comparator output goes positive and (via the filter network) causes the VCO frequency to increase until both its frequency and phase precisely match (phase lock with) those of the external signal. If the VCO frequency rises above that of the external signal the reverse action takes place, and the comparator output goes low and makes the VCO frequency decrease until it finally locks to that of the external signal. Thus, this circuit causes the VCO signal to automatically phase lock to the external input signal.

Note that in the above tracking circuit the VCO generates a clean (noise-free) and symmetrical output waveform, even if the input signal is noisy and non-symmetrical, and that (because the low-pass filter has a finite time constant) the VCO tracks the *mean* phase and frequency of the input signal. It can thus be used to track and clean up slowly varying input signals, or to track

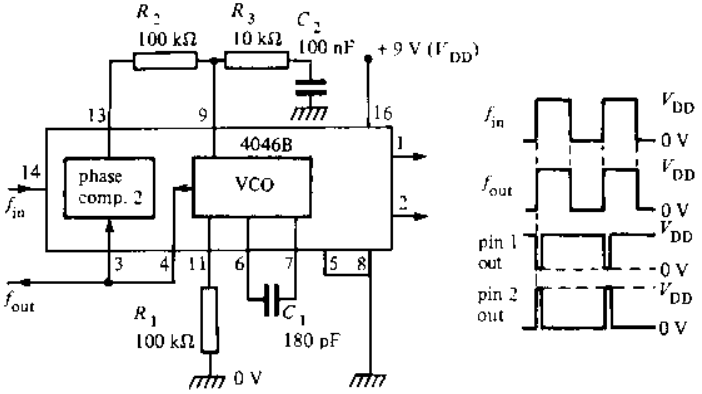

Figure 10.19 *Wide-range PLL signal tracker, showing waveforms obtained when the loop is locked*

the centre frequency of an FM signal and provide a demodulated signal at the comparator output.

Figure 10.19 shows how the 4046B can be used as a practical wide-range PLL that will capture and track any input signal within the 100 Hz to 100 kHz (approximate) span range of the VCO, provided that the pin 14 input signal switches fully between the logic-0 and logic-1 levels. Filter R_2-R_3-C_2 is used here as a sample-and-hold network, and its component values determine the settling and tracking times of signal capture. The VCO frequency is controlled by C_1-R_1 and the pin 9 voltage; the VCO span range (and thus the capture and tracking range of the circuit) varies from the frequency obtained with pin 9 at zero volts to that obtained with pin 9 at full supply rail value.

Figure 10.20 shows a lock detector/indicator that can be used with the above PLL circuit. The operating principle of this detector is moderately

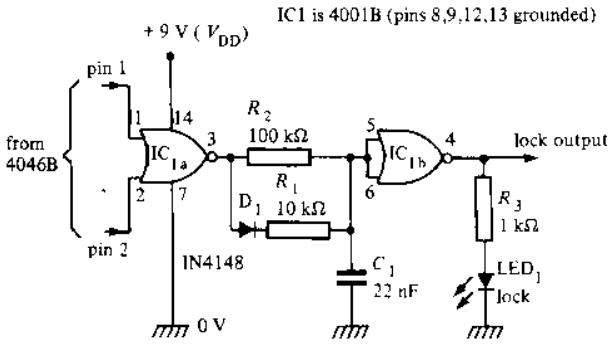

Figure 10.20 *PLL lock detector/indicator*

complex. Within the 4046B IC the output of each of the two phase comparators comprises a series of pulses with widths proportional to the difference between the two input signals of the comparator. When the PPL circuit is locked (see *Figure 10.19*) these two outputs are almost perfect mirror images of each other; when the loop is not locked the signals are greatly different. In *Figure 10.20* these two outputs are fed to the inputs of NOR gate IC_{1a}. The circuit action is such that when the loop is locked the IC_{1a} output is permanently low and illuminates LED_1 via IC_{1b}, but when the loop is not locked the output of IC_{1a} comprises a series of pulses that rapidly charge C_1 via D_1-R_1 and thus drive IC_{1b} output low and turn LED_1 off.

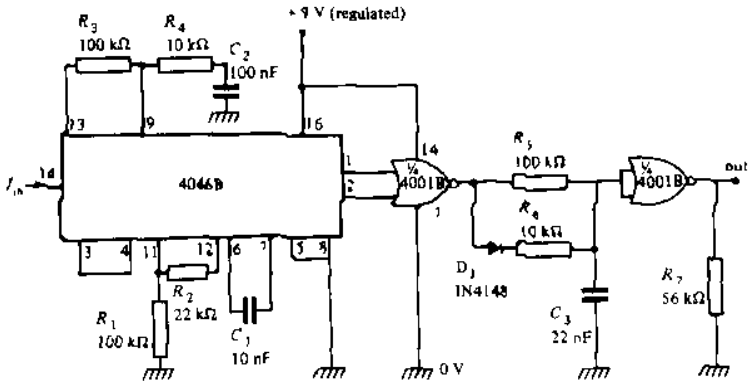

Figure 10.21 *Precision narrowband 1.8 kHz to 2.2 kHz tone switch*

Figure 10.21 shows how a PLL circuit can be combined with the above lock indicator to make a precision narrowband tone switch. In this case the maximum VCO frequency is determined by C_1-R_1, and the minimum by C_1 and $R_1 + R_2$. The frequency is variable from about 1.8 kHz to 2.2 kHz with the component values shown, and the circuit can thus only lock to signals within this frequency range. The circuit output is normally low, but switches high when locked to a suitable input signal.

Frequency synthesis

One of the most useful applications of the PLL is as a frequency multiplier or synthesizer. *Figure 10.22* shows the basic principle. This circuit is similar to that of the basic PLL (*Figure 10.18*) circuit, except for the addition of the divide-by-N counter between the VCO output and the phase comparator input. The circuit action is such that the VCO frequency automatically locks to a value at which the divider output frequency matches that of the external

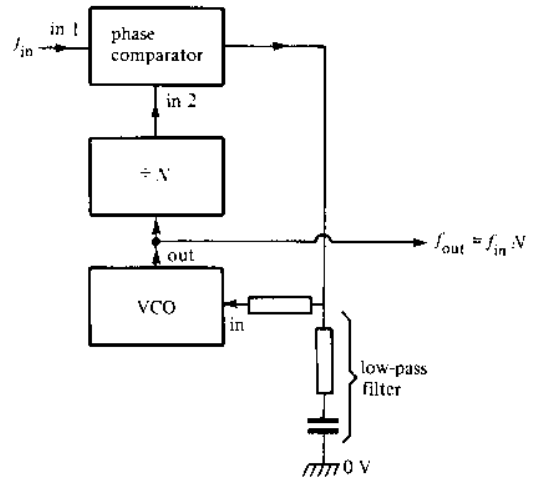

Figure 10.22 *Basic frequency synthesizer or multiplier circuit*

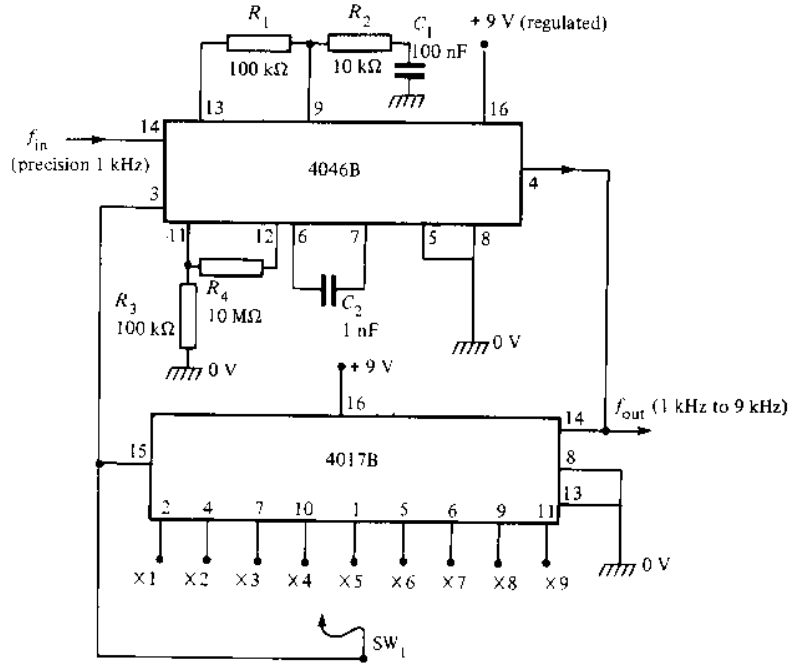

Figure 10.23 *Simple 1 kHz to 9 kHz frequency synthesizer*

input signal, and under this condition the VCO frequency is obviously N times the input frequency (where N is the counter's division ratio). If the input signal is derived from a precision crystal source, output signals of equal precision can thus be synthesized at any desired multiple frequency by simply using a divider with a suitable N value.

Figure 10.23 shows a practical example of a simple frequency synthesizer. It is fed with a precision (crystal-derived) 1 kHz input signal, and provides an output that is a whole-number multiple (in the range × 1 to × 9) of this signal. The 4017B is used as a programmable divide-by-N counter in this simple application, but can easily be replaced by a string of programmable decade down counters of the type described in Chapter 9, to make a wide-range (10 Hz to 1 MHz) synthesizer.

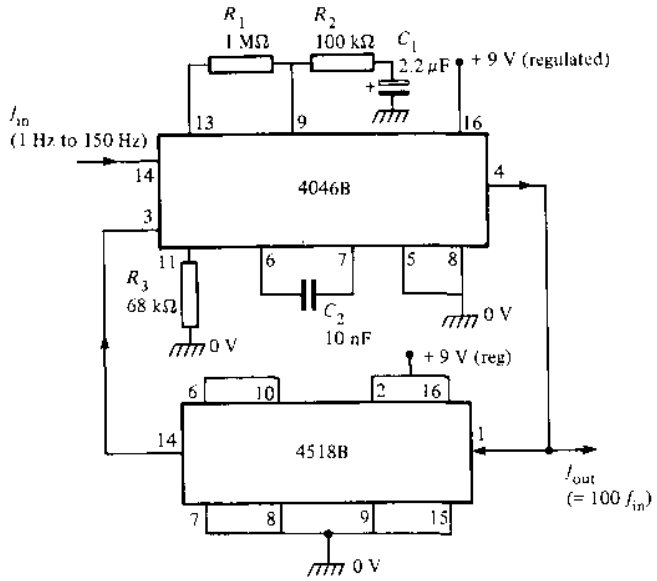

Figure 10.24 *A × 100 low-frequency prescaler*

Finally, to complete this volume, *Figure 10.24* shows how the synthesizer principle can be used to make a × 100 frequency prescaler that can be used to change a hard-to-measure 1 Hz to 150 Hz input signal into a 100 Hz to 15 kHz output signal that can easily be measured on a standard frequency counter. The 4518B IC used in this circuit actually contains a pair of decade counters, and in *Figure 10.24* these are cascaded to make a divide-by-100 counter.

from about 4 kΩ to 22 MΩ; C_1 is the time-constant capacitor and can have any value from a few picofarads to many hundreds of microfarads, and may be of the polarized or non-polarized types.

The astable circuit can only work if pin 4 is tied to the positive supply rail; if pin 4 is grounded, the astable is disabled. The astable can thus be used in the gated mode by simply wiring pin 4 as shown in *Figure 5.23*.

The basic astable circuit generates an almost symmetrical output waveform. It can be made to generate a non-symmetrical waveform in a variety of ways. *Figure 5.24* shows one useful variation. In this case C_1

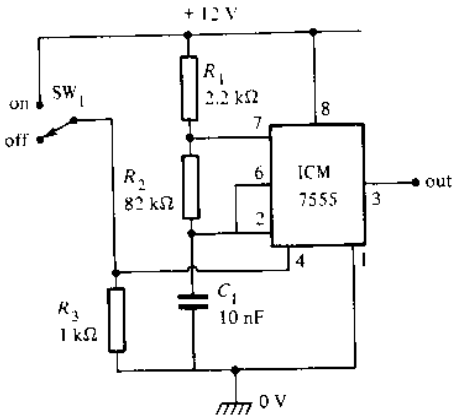

Figure 5.23 *Gated 7555 astable*

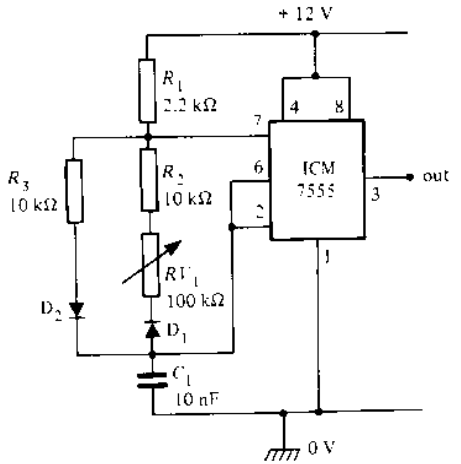

Figure 5.24 *Astable with variable M:S ratio*

alternately charges via R_1-R_3 and D_2, and discharges via D_1-RV_1 and R_2; the output waveform symmetry of this circuit is thus fully variable via RV_1.

4046B VCO circuits

To complete this look at CMOS square-wave and clock generator circuits, let's consider some practical VCO (voltage-controlled oscillator) applications of the 4046B phase-locked-loop (PLL) IC. *Figure 5.25* shows the internal block diagram and pin-outs of this chip, which contains a couple of phase comparators, a VCO, a zener diode, and a few other bits and pieces.

For our present purpose, the most important part of the chip is the VCO section. This is a highly versatile device. It produces a well-shaped symmetrical square-wave output, has a top-end frequency limit in excess of 1 MHz, has a voltage-to-frequency linearity of about 1 per cent and can easily be scanned

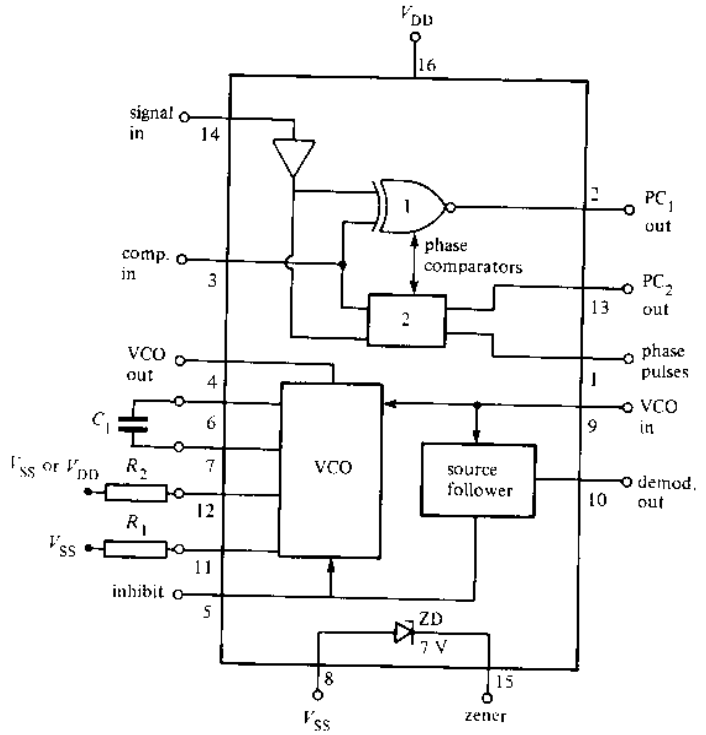

Figure 5.25 *Internal block diagram and pin-outs of the 4046B*

through a 1 000 000:1 range by an external voltage applied to the VCO input terminal. The frequency of the oscillator is governed by the value of a capacitor (minimum value 50 pF) connected between pins 6 and 7, by the value of a resistor (minimum value 10 kΩ) wired between pin 11 and ground, and by the voltage (any value from zero to the supply voltage value) applied to VCO input pin 9.

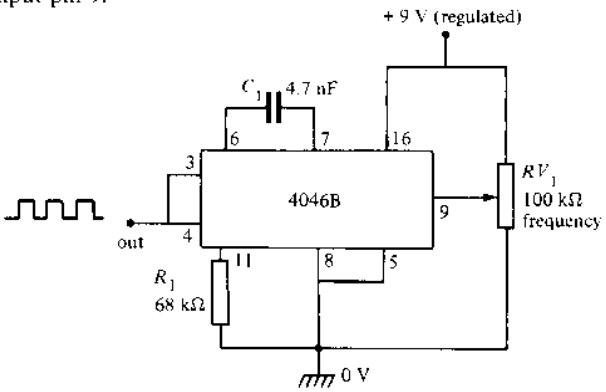

Figure 5.26 *Basic wide-range VCO, spanning near-zero to roughly 5 kHz via* RV_1.

Figure 5.26 shows the simplest possible way of using the 4046B VCO as a voltage-controlled square-wave generator. Here, C_1-R_1 determines the maximum frequency that can be obtained (with the pin 9 voltage at maximum) and RV_1 controls the actual frequency by applying a control voltage to pin 9: the frequency falls to a very low value (a fraction of a hertz)

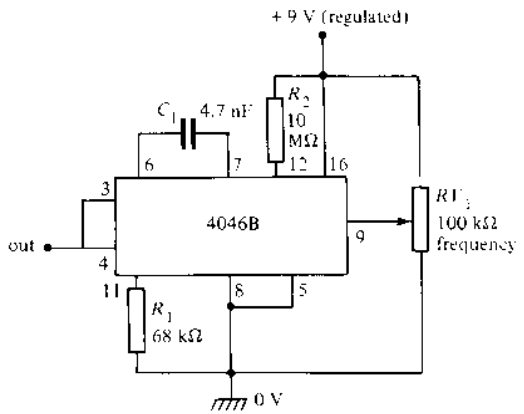

Figure 5.27 *The frequency of this VCO is variable all the way down to zero*

with pin 9 at zero volts. The effective voltage-control range of pin 9 varies from roughly 1 V below the supply value to about 1 V above zero, and gives a frequency span of about 1 000 000:1. Ideally, the circuit supply voltage should be regulated.

It was stated above that the frequency falls to near-zero when the input voltage of the *Figure 5.26* circuit is reduced to zero. *Figure 5.27* shows how the circuit can be modified so that the frequency falls all the way to zero with zero input, by wiring high-value resistor R_2 between pins 12 and 16. Note here that, when the frequency is reduced to zero, the VCO output randomly settles in either a logic-0 or a logic-1 state.

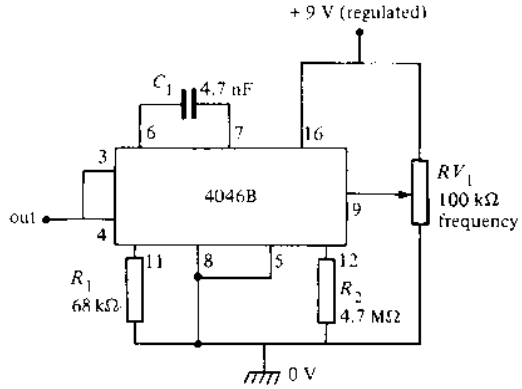

Figure 5.28 *Restricted-range VCO, with frequency variable from roughly 72 Hz to 5 kHz via* RV_1.

Figure 5.28 shows how the pin 12 resistor can alternatively be used to determine the minimum operating frequency of a restricted-range VCO. Here, f_{min} is determined by C_1-R_2, and f_{max} is determined by C_1 and the parallel resistance of R_1 and R_2.

Figure 5.29 shows an alternative version of the restricted-range VCO in which f_{max} is controlled by C_1-R_1, and f_{min} is determined by C_1 and the series combination of R_1 and R_2. Note that, by suitable choice of the R_1 and R_2 values, the circuit can be made to span any desired frequency range from 1:1 to near-infinity.

Finally, it should be noted that the VCO section of the 4046B can be disabled by taking pin 5 of the package high (to logic-1) or enabled by taking pin 5 low (to logic-0). This feature makes it possible to gate the VCO on and off via external signals. Thus, *Figure 5.30* shows how the basic VCO circuit can be gated via a signal applied to an external inverter stage. Alternatively, *Figure 5.31* shows how one of the internal phase comparators of the 4046B can be used to provide gate inversion, so that the VCO can be gated via an external voltage applied to pin 3.

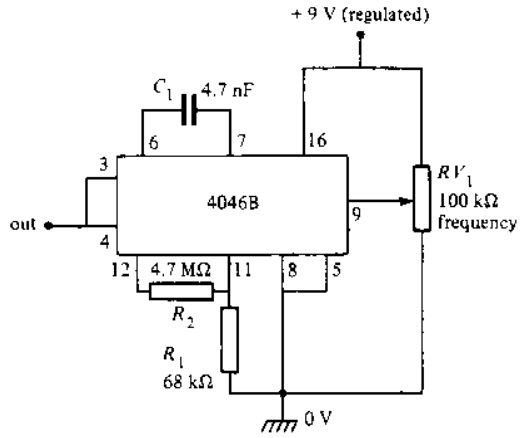

Figure 5.29 *Alternative version of the restricted-range VCO.* f_{max} *is controlled by* C_1-R_1, f_{min} *by* C_1-$(R_1 + R_2)$

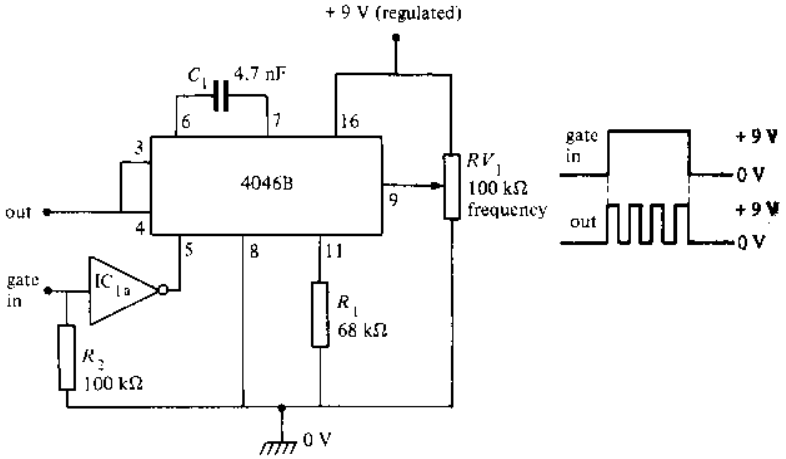

Figure 5.30 *Gated wide-range VCO, using an external gate inverter*

Bistable circuits

Strictly speaking, a clock generator can be any circuit that generates a clean (noiseless, with sharp leading and trailing edges) waveform suitable for clocking modern fast digital counter/divider circuitry. Thus a clock generator can take the form of a simple Schmitt trigger that converts a sine-wave input into a good square-wave output, or a square-wave generator of the type

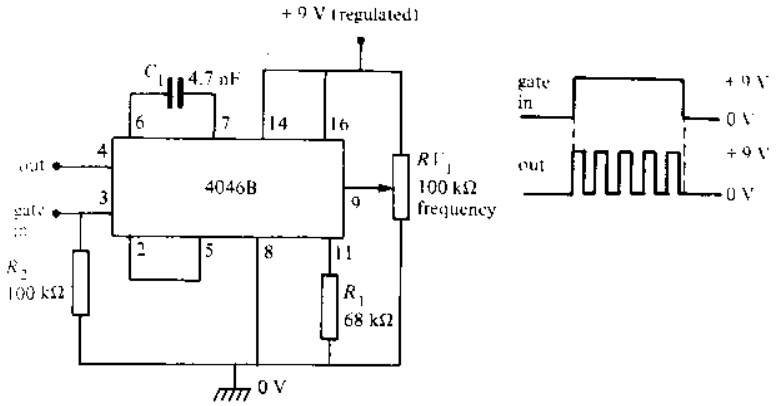

Figure 5.31 *Gated wide-range VCO, using one of the internal phase comparators as a gate inverter*

already described in this chapter, or of a monostable pulse generator of the type described in chapter 6, and so on.

One particularly useful type of clock generator is the simple R-S (reset-set) bistable (also known as the R-S flip-flop), which can be used to deliver a single clock pulse each time the available one of its two input terminals is activated, either electronically or via a push-button switch. *Figures 5.32* to *5.35* show four ways of making such bistables, using pairs of 4001B or 4011B gates.

The bistable circuit of *Figure 5.32* is triggered by positive-going input pulses, and is designed around 4001B NOR-type gates. *Figure 5.33* shows how the circuit can be modified for push-button triggering.

The bistable circuit of *Figure 5.34* is triggered by negative-going input pulses, and is designed around 4011B NAND-type gates. *Figure 5.35* shows the circuit modified for push-button triggering.

Note that, in all the above circuits, once the bistable has been set its state

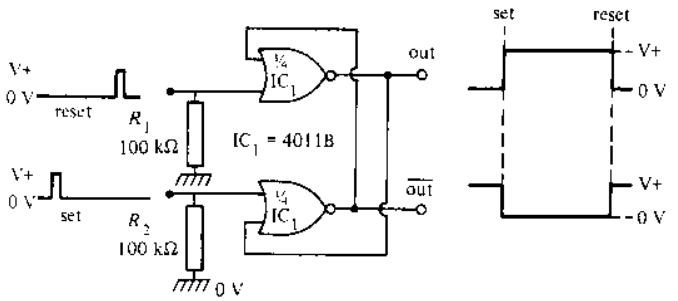

Figure 5.32 *Pulse-triggered NOR bistable*